IN THE CLAIMS

This listing of the claim will replace all prior versions and listings of claim in the present application.

Listing of Claims

Claims 1-4 (canceled).

5. (currently amended)A packet switching system, comprising:

a plurality of input line processors;

a plurality of output line processors;

a plurality of input buffers including a plurality of queue buffers, being provided corresponding to the output line processors, and being connected to the input line processors;

a crossbar switch being connected to the input buffers and the output line processors;

an arbiter to arbitrate for assigning grant of transmitting a packet to said crossbar switch, to any of queue buffers of the queue buffers; and

means to determine priority as a parameter between an interval of time for a packet to be transmitted to the crossbar switch from said queue buffer and a queue length of said queue buffer, both are calculated for each queue buffer of said queue buffers, to thereby select a queue buffer among all queue buffers in the input buffers and give the selected queue the grant for transmitting a packet to said crossbar switch;

wherein said arbiter performs arbitration according to said priority determined on all queue buffers of the input buffers; and

wherein the arbitration is performed based on a transmit priority level calculated by the equation of L=1n(M-a*t/b*sXe), where L is the priority level, M is the time out, t is output data interval, s is the number of segments at present time, a is output data coefficient, and b is queue length coefficient.

6. (original) A packet switching system as set forth in Claim 5, further comprising:

output data interval measuring means for measuring an interval of time for a packet to be transmitted to the crossbar switch from said queue buffer, and

queue length measuring means for measuring a length of the queue buffer, both measuring each queue buffer of all the queue buffers.

7. (original) A packet processing unit as set forth in Claim 5, wherein the arbitration is performed by taking as a parameter the queue length prior to the time interval so as to prevent packets from overflowing from each of the queue buffers.

8. (original) A packet processing unit as set forth in Claim 5, wherein the arbitration is performed by taking as a parameter the time interval prior to the queue length, so as to shorten a time for a packet to exist in each of the queue buffers.

9. (new) A packet switching system, comprising:

a plurality of input line processors;

a plurality of output line processors;

a plurality of input buffers including a plurality of queue buffers, being provided corresponding to the output line processors, and being connected to the input line processors;

a crossbar switch being connected to the input buffers and the output line processors;

an arbiter to arbitrate for assigning grant of transmitting a packet to said crossbar switch, to any of queue buffers of the queue buffers;

means to determine priority as a parameter between an interval of time for a packet to be transmitted to the crossbar switch from said queue buffer and a queue length of said queue buffer, both are calculated for each queue buffer of said queue buffers, to thereby select a queue buffer among all queue buffers in the input buffers and give the selected queue the grant for transmitting a packet to said crossbar switch,

wherein said arbiter performs arbitration according to said priority determined on all queue buffers of the input buffers;

priority level collector for collecting a priority level of each of queue buffers included in the input buffer;

input tournament processor for determining the highest level buffer from the collected levels of the same input line; and

output tournament processor for determining the highest level buffer from the collected levels of the same input line,

wherein arbitration is performed by re-assigning the priority level based on the process result of the input tournament processor and output tournament processor.

10. (new) A packet switching system according to claim 9, wherein the re-assignment is performed by:

a step of dividing the buffers in the most high priority level or a group of the most high priority level, and a group of others;

a step of assigning a first high priority level to the buffer whose both of priority level of input and output lines is the most high;

a step of assigning the first high priority level to the buffer whose one of priority level of input or output lines is in the highest group, and the other is the highest;

a step of assigning a second high priority level to the buffer whose both of priority level of input and output lines are in the highest group;

a step of assigning a third high priority level to the buffer whose one of priority level of input or output line is in the highest group, and the other is in the group of others; and

a step of assigning a fourth high priority level to the buffer whose both of priority level of input and output lines are in the group of others.